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Tutorial #1

Cross-Layer Soft-Error Resilience Analysis of Computing Systems

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Part #2

Device Level Resilience

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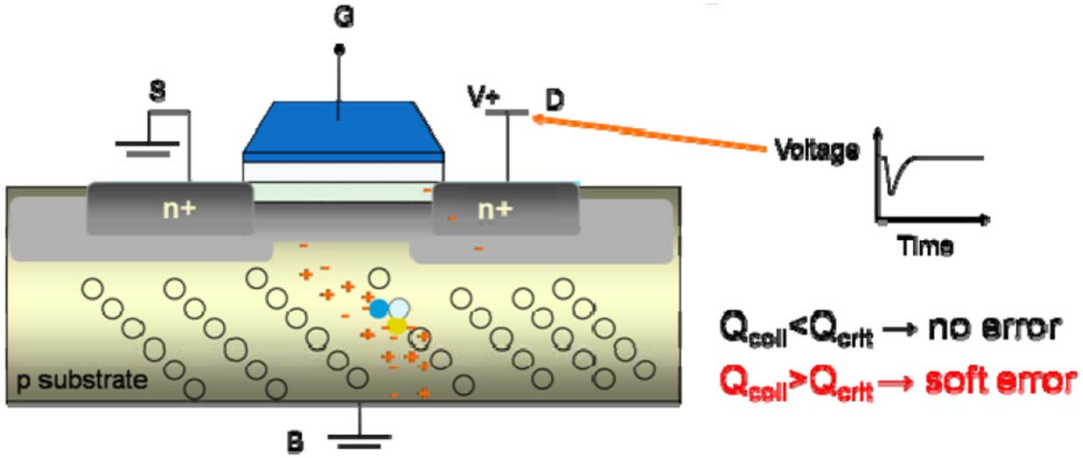
Agenda

- Key technological aspects
- Fault injection at the device level taxonomy
  - Physics approaches (i.e. beaming)
  - Simulation/Emulation approaches (transistor and circuit level)
  - Analytical approaches (at the circuit level)
- State-of-the art TVF
- Summary and conclusions

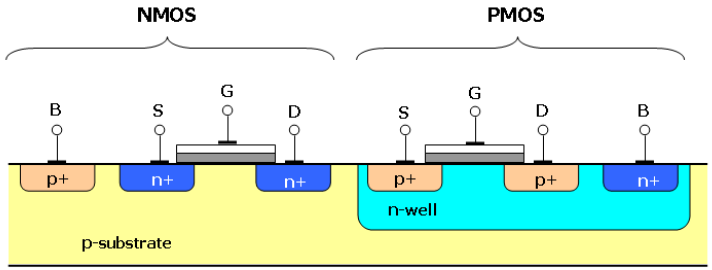
Key Technological Aspects

- Collected charge, Q critical
  - If Charge Collected (Qcoll) by a particle is greater than Qcrit a soft error is produced
  - Charge Collection Efficiency (Qs) is the mean of Qcoll in a range of energy particles
  - Qs is a parameter dependent of the technology that is usually computed experimentally
  - Qs is usually scaled down from experimental data.

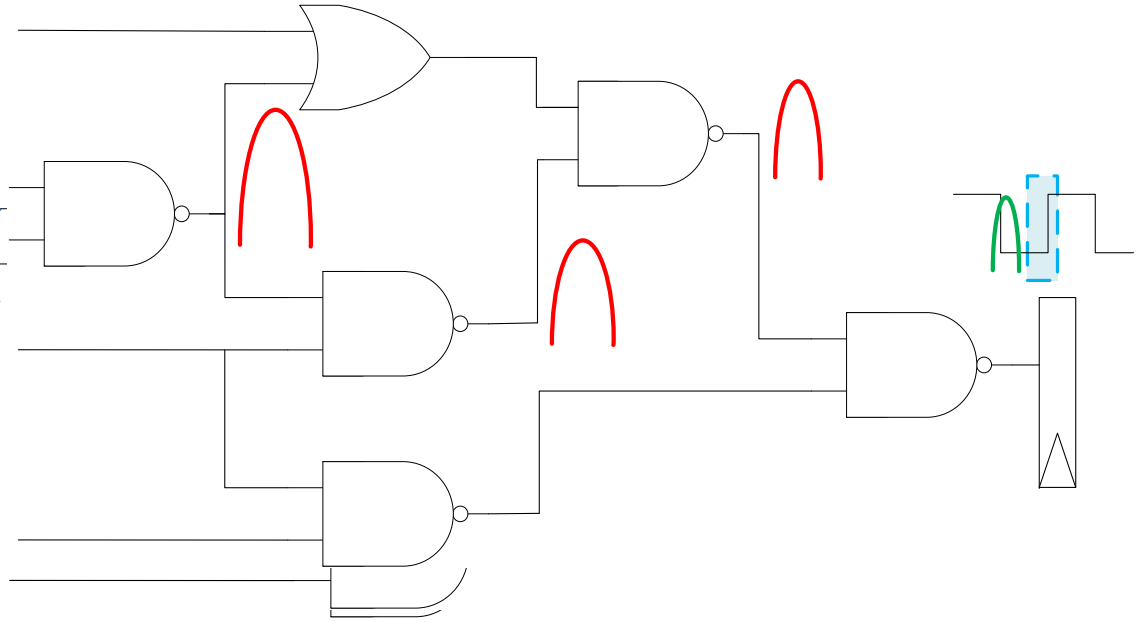


Key Technological Aspects

- Well boundary
  - Particle strikes hardly cross well boundaries



- Masking factors
  - Logical
  - Electrical
  - Temporal

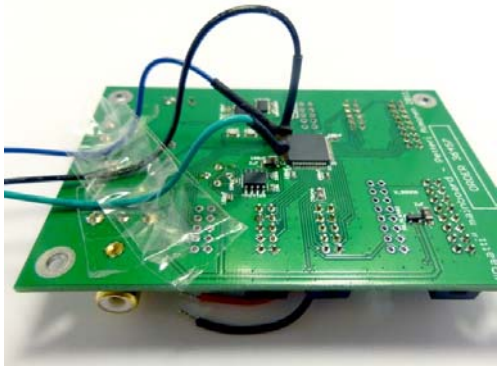


Taxonomy

- Beaming (simulation)
- Software Simulation
  - Device/circuit level – Spice
  - Circuit level – VHDL, Verilog
- Software Emulation
  - HDL+FPGA
- Analytical (software)
  - Custom software

Taxonomy - Beaming

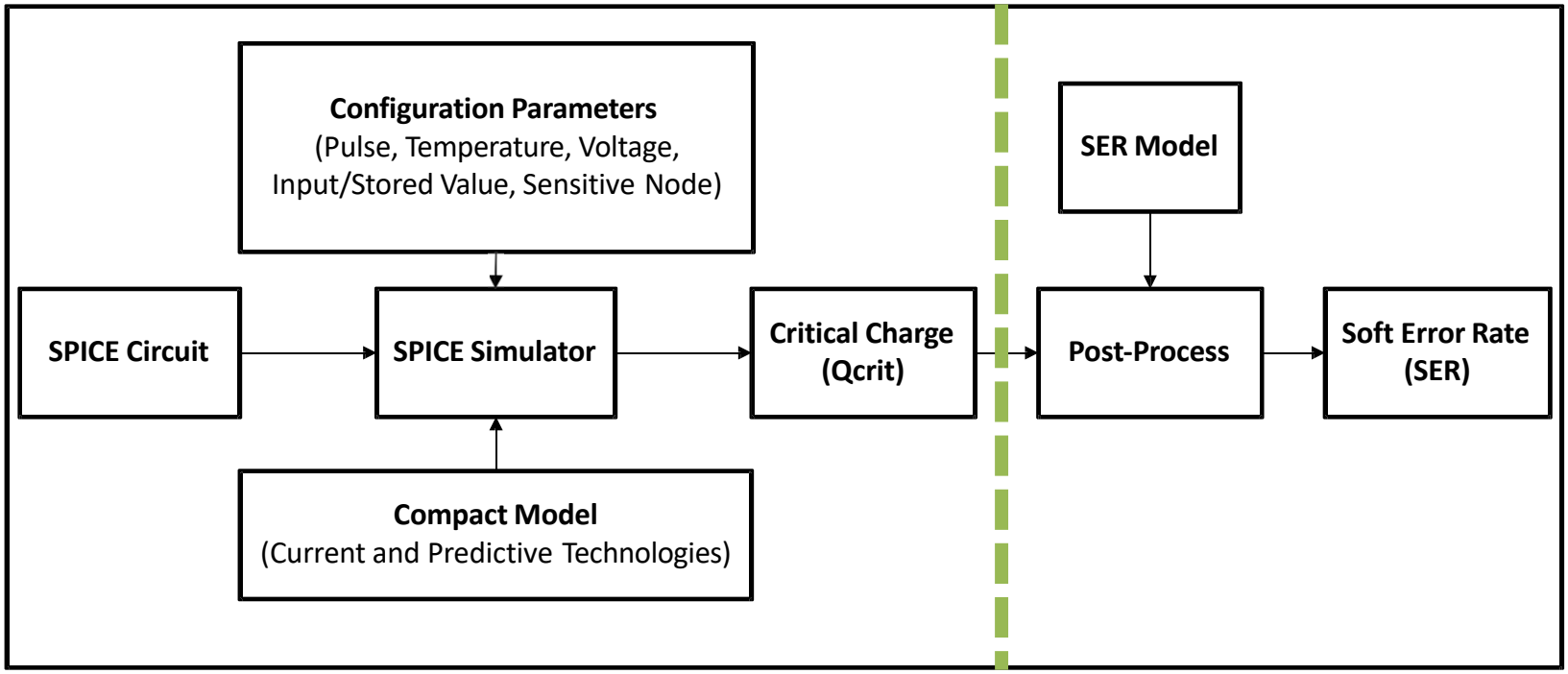
- Contact based: an external interface of the integrated circuit is perturbed (i.e. pin-level active probes and socket insertion)



- Non-contact based: a parts of the chip is bombarded with an external energy source (i.e. beams of laser, heavy ions, protons, and neutrons)

Taxonomy – Software Simulation - Spice

- Spice

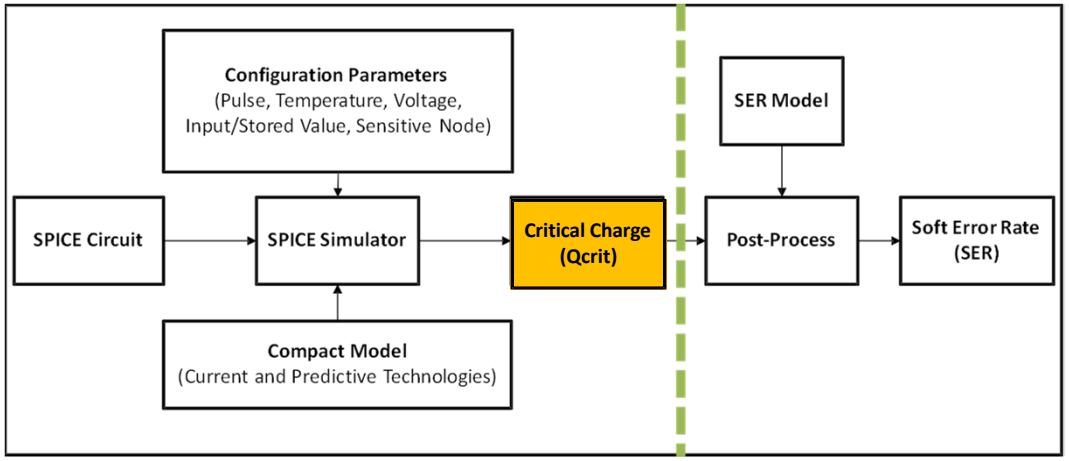


Taxonomy – Software Simulation - Spice

- Critical Charge computation
  - Qcrit is the minimum charge needed to cause a bit flip
  - Qcrit is computed with SPICE by injecting a current pulse in the sensitive nodes
  - A double exponential pulse is most used:

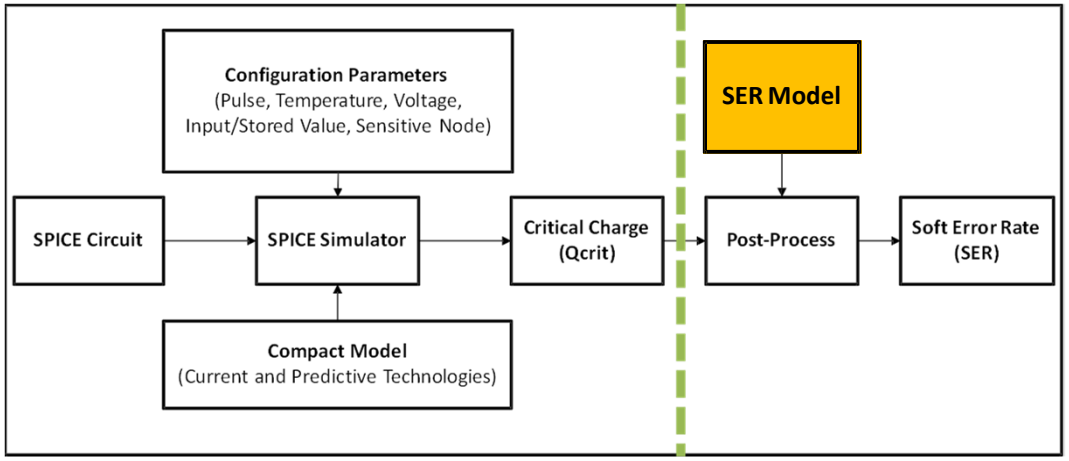
$$I(t) = (Q/(rf - rr)\,[\exp(-t/rf) - \exp(-t/rr)]$$

  - Factors that impact Qcrit:
    - Supply Voltage, temperature



Taxonomy – Software Simulation - Spice

- SER computation
  - The model of Hazucha and Svensson is generally used:
    - $SER = K \cdot Flux \cdot Area \cdot e^{-Qcrit/Qs}$



K: Constant (Technology independent parameter)
Flux: Reference Neutron Flux from NYC
Area: Sensitive Area to neutron strikes
Qs: Charge Collection Efficiency (Technology dependent parameter)
Qcrit: Critical Charge
Qcrit and Area can be easily computed but K and Qs are derived empirically
K is technology independent so the value provided by Hazucha can be used

-Other models available: Burst Generation Rate (BGR), Neutron Cross-Section (NCS)

Taxonomy – Simulation - Spice

- Spice-like simulators
  - Methodology well-known
  - Any circuit/technology available can be analyzed

+ Open source versions of Spice
+ All masking factors included
– Can be slow for large circuits
– Needs minimal VLSI knowledge

Taxonomy – Simulation - HDL

- Verilog or VHDL
  - Use simulator capabilities to switch values
  - Force/Release statements
  - PLI/VPI extensions

  \+ Faster than Spice

  \+ Logic and timing masking analysis

  – No electrical masking

Taxonomy - Emulation

- Emulation
  - HDL+FPGA
  - Insert hand-made fault injector block

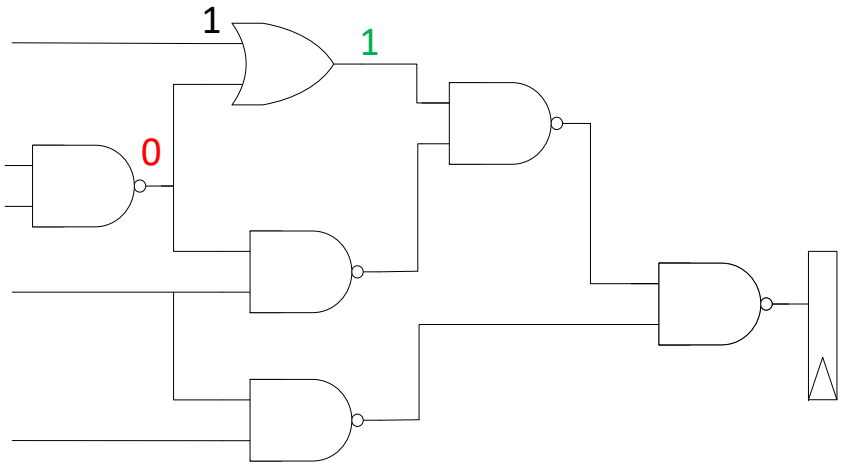
+ Faster than simulation

+ Logic and timing masking analysis

~ electrical masking (cumbersome to model different pulses)

Taxonomy - Analytical

- Analytical
  - Based on graph algorithms representing the netlist
  - MUST take care of reconvergence
  - MUST accommodate all kinds of masking



+ Faster than simulation/emulation

+ Logic, electrical and timing masking analysis

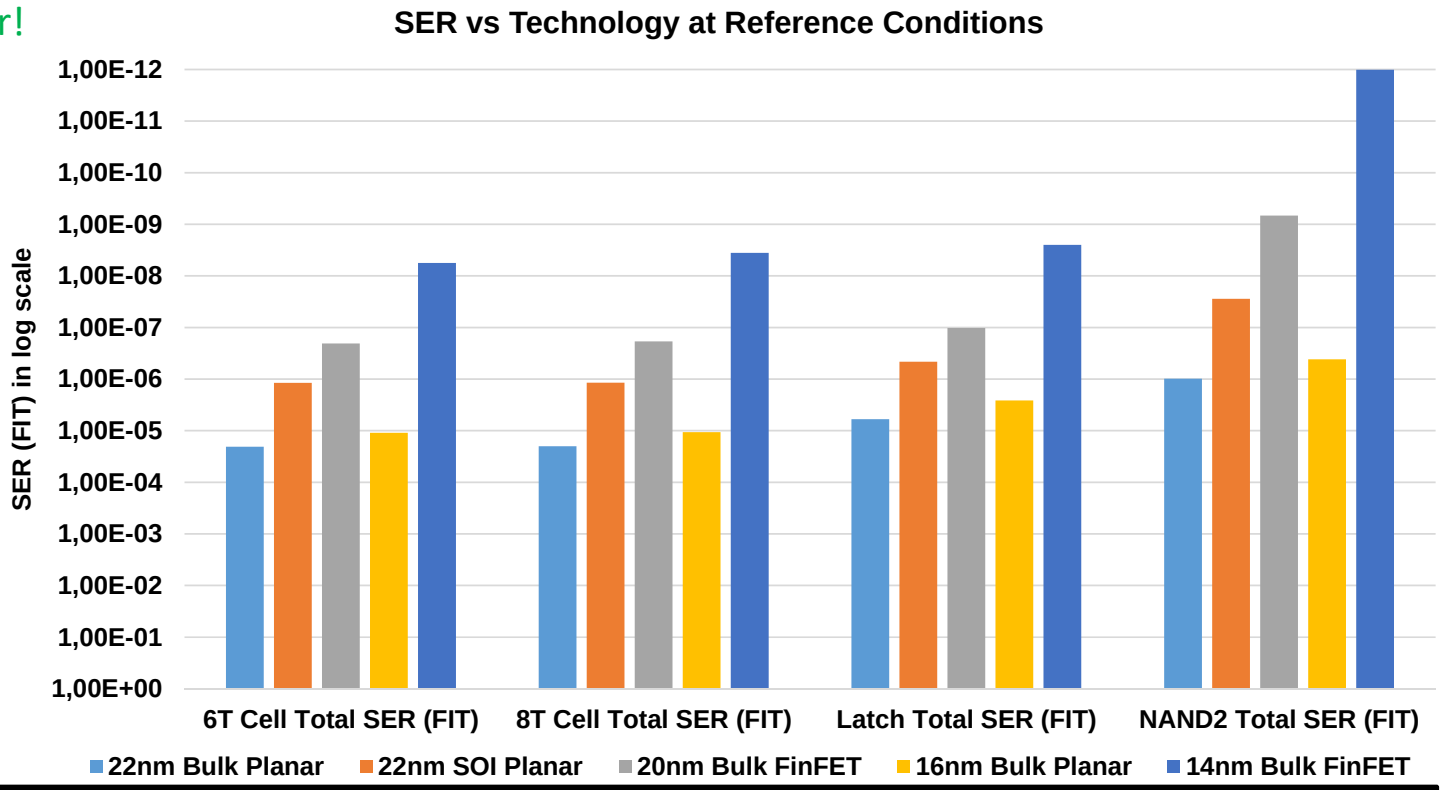
~ tradeoff speed vs. accuracy

Taxonomy - Summary

	Beaming	Spice	HDL sim	HDL emu	Analytical
Target	Manufactured circuit	Device, small circuit	Circuit	Circuit	Circuit
Cost tools	$$$	0	0	$	0
Simulation speed	High	Low	Low	Medium	High
Accuracy	High	High	Medium	Medium	Medium/Low

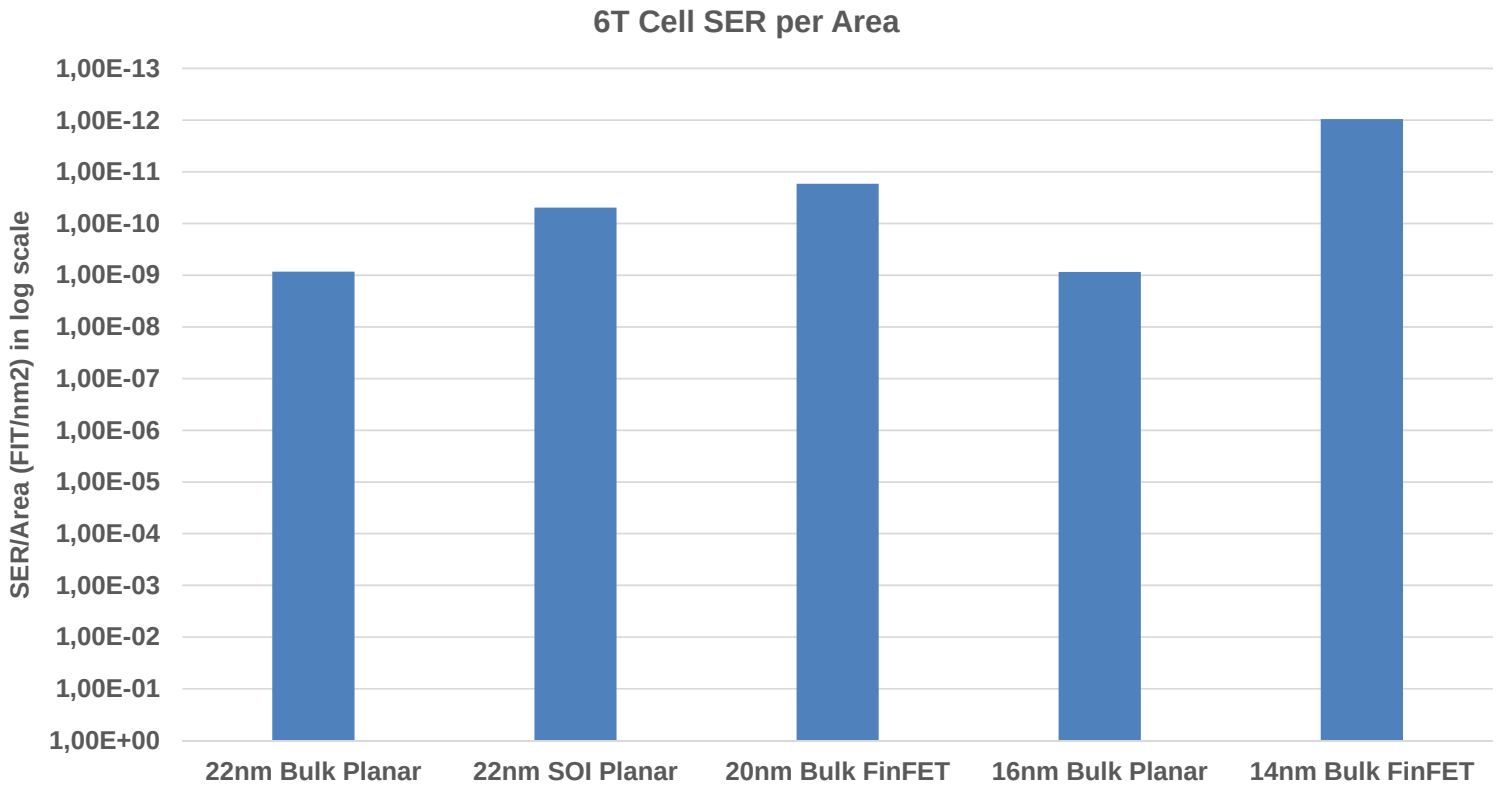
State-of-the art TVF (blocks and tech nodes)

Higher is better!



"*A Detailed Methodology to Compute Soft-Error Rates in Advanced Technologies*",
M. Riera, R. Canal, J. Abella, A. Gonzalez, DATE'16, March 2016

State-of-the art TVF (iso-area)



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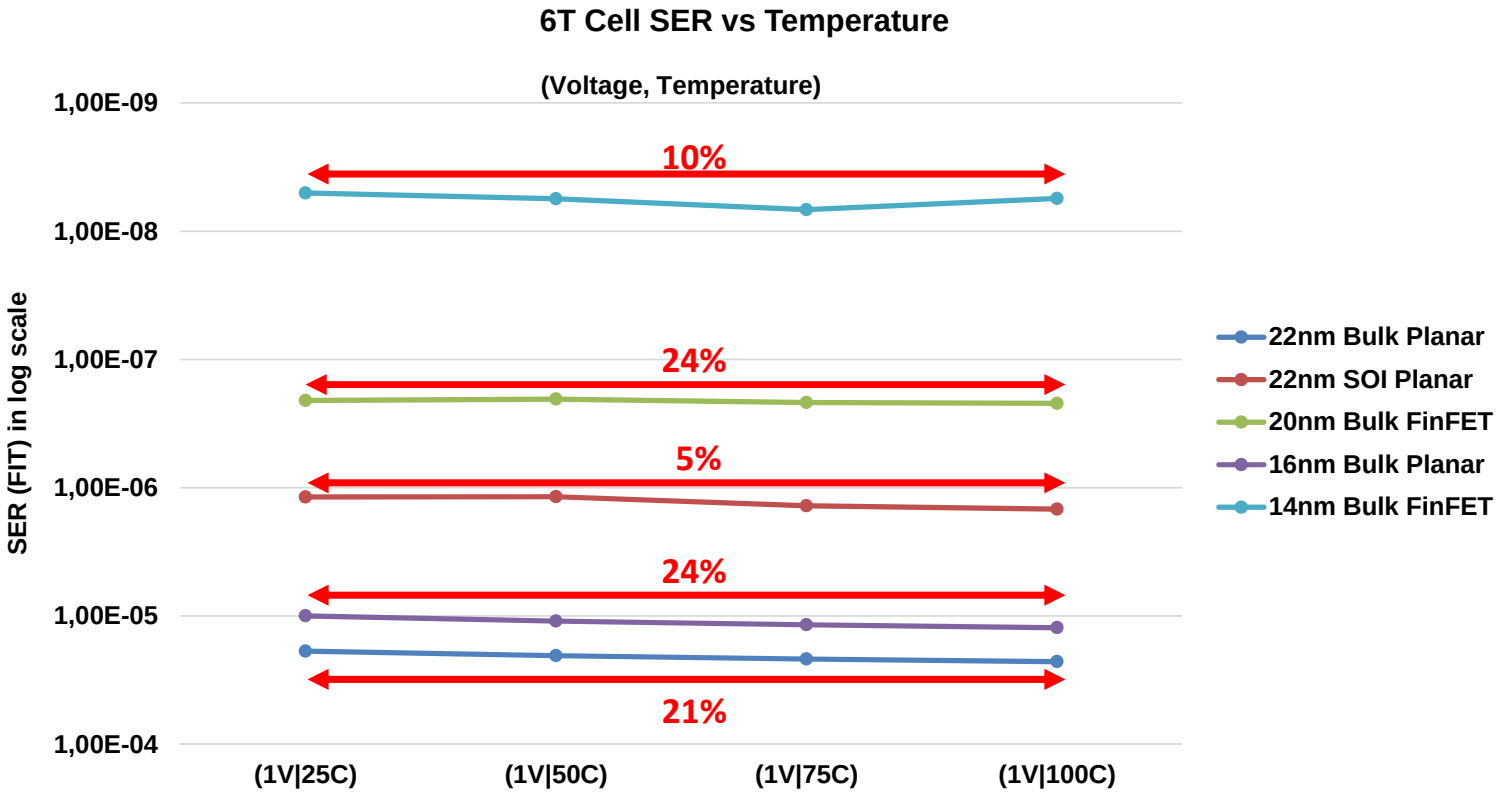
M. Riera, R. Canal, J. Abella, A. Gonzalez, DATE'16, March 2016

State-of-the art TVF (Temperature trends)



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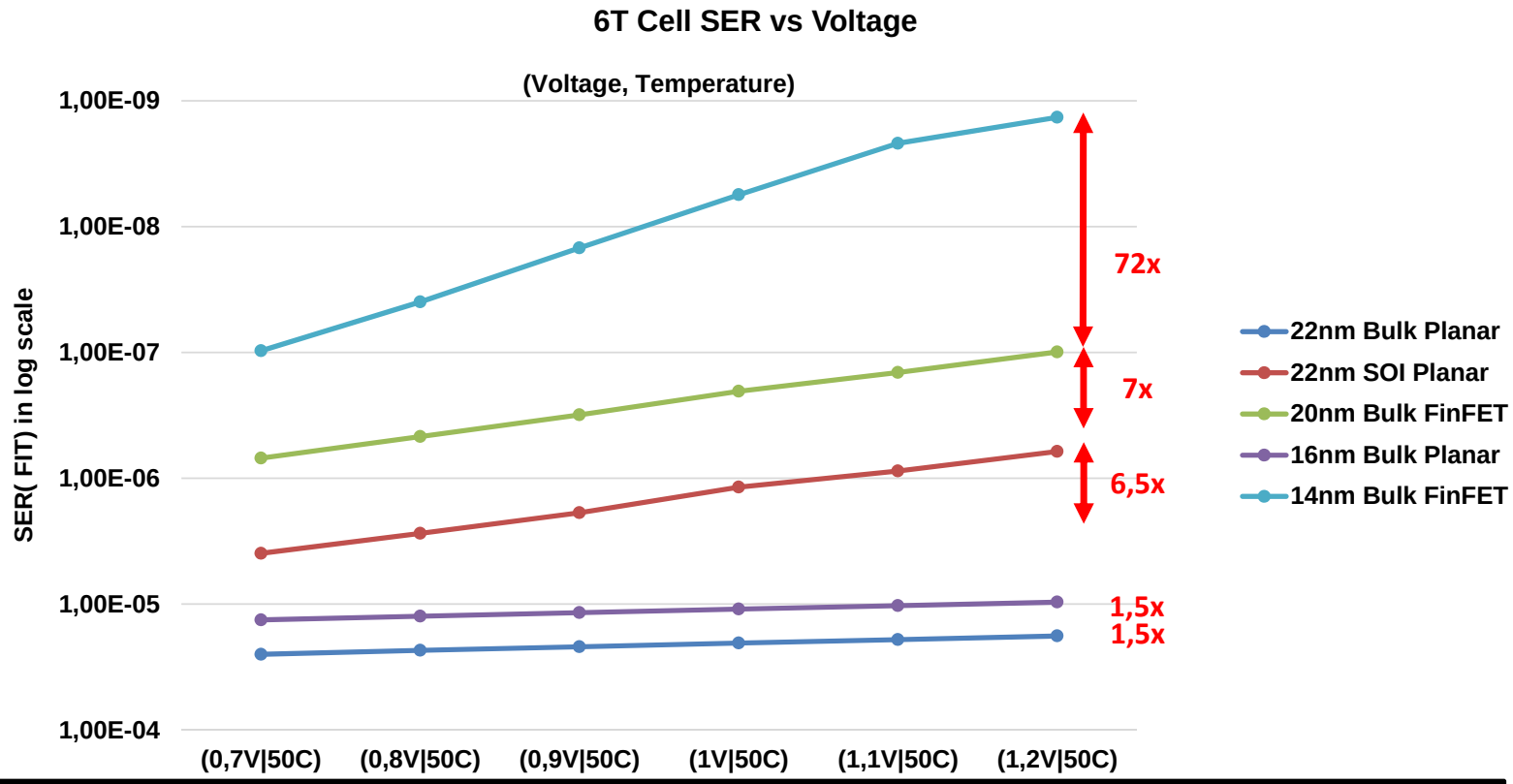
M. Riera, R. Canal, J. Abella, A. Gonzalez, DATE'16, March 2016

State-of-the art TVF (Voltage trends)



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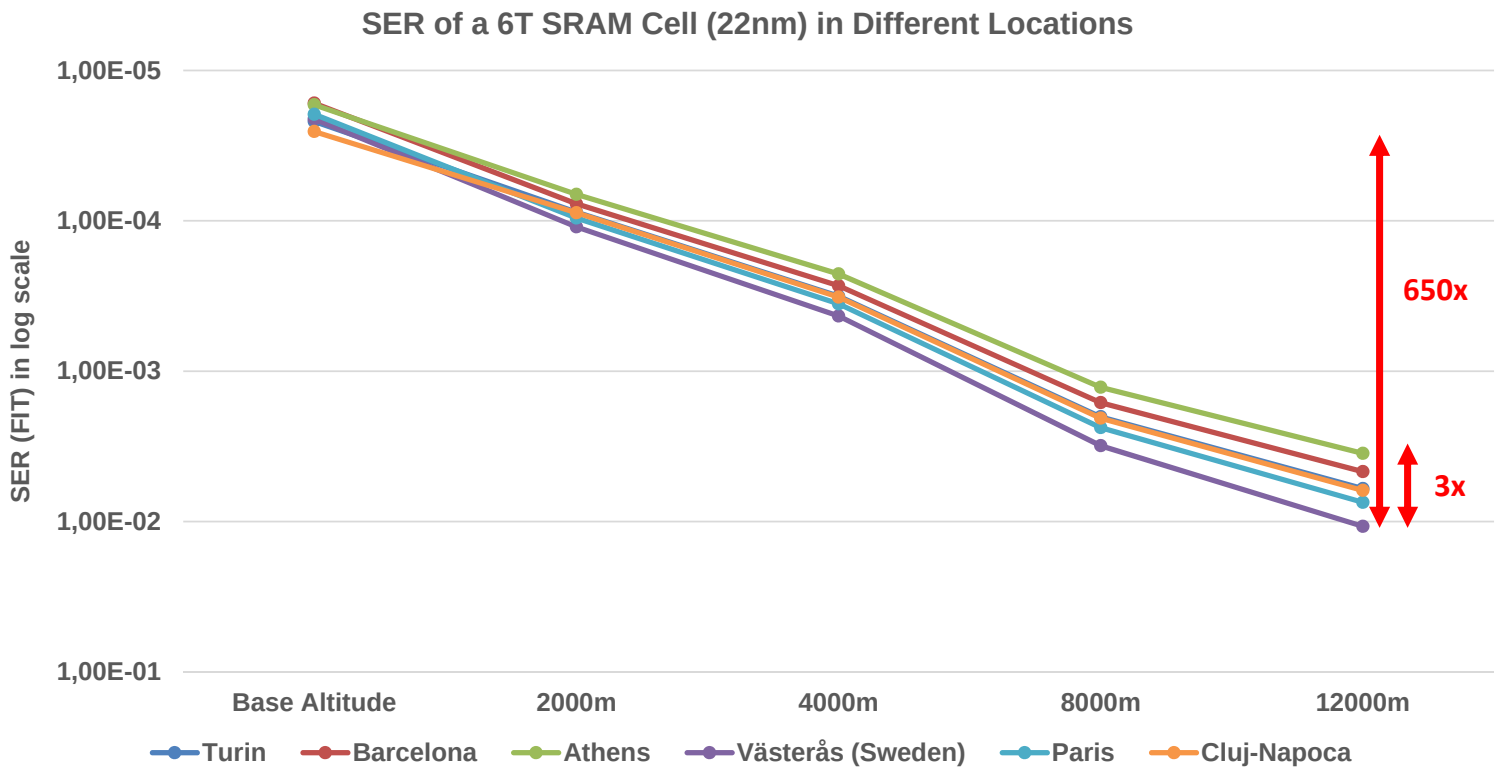
State-of-the art TVF (location and altitude)



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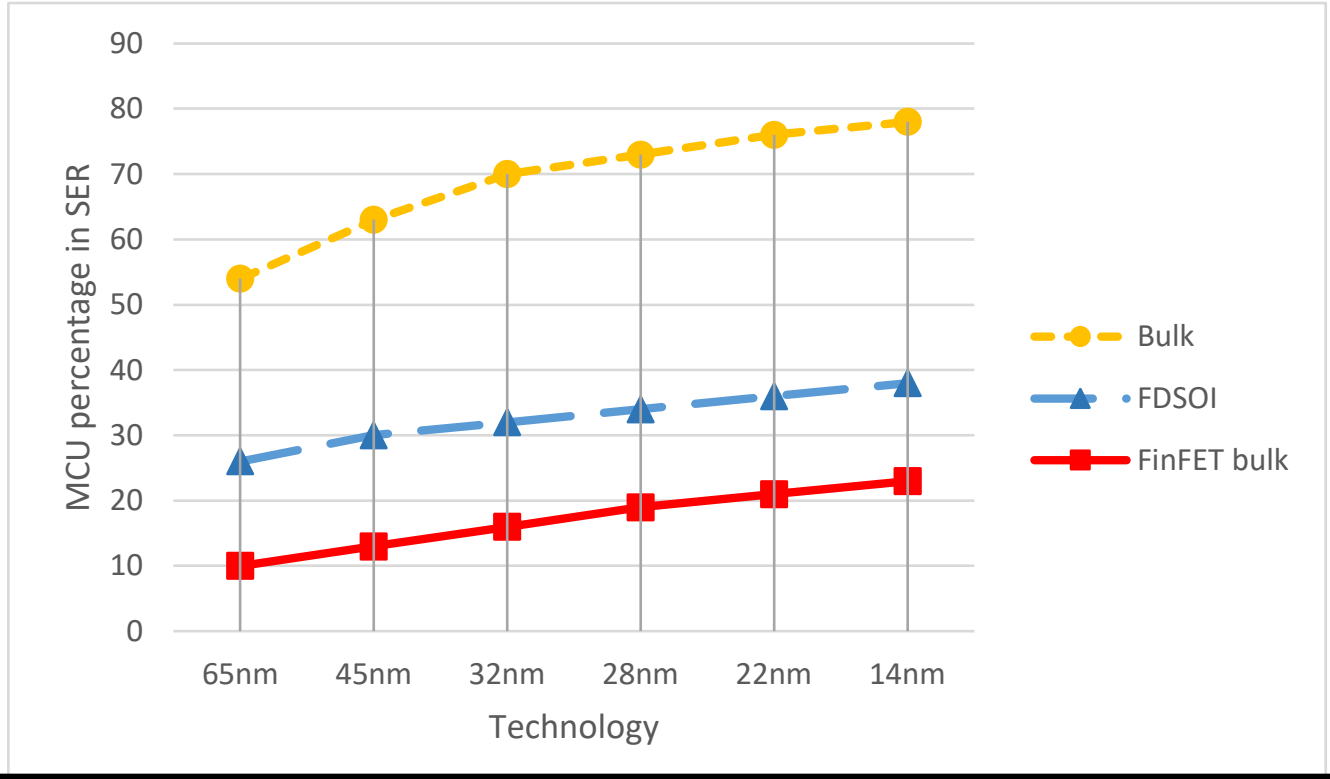
M. Riera, R. Canal, J. Abella, A. Gonzalez, DATE'16, March 2016

State-of-the art TVF (summary)

- Bulk planar is becoming more vulnerable to soft errors:
  - Lower nodes increases the total SER since more components are introduced
- New technologies and materials can improve the reliability of the device:
  - Bulk FinFET reduces SERs up to 100x
  - SOI Planar reduces SERs up to 20x
- Environmental parameters and location also have a huge impact on SERs:
  - SERs can vary from 1,2x to 70x due temperature and voltage, with a stronger effect of voltage
  - SERs can increase up to 650x due the altitude

State-of-the art TVF (extra on multi-cell upsets)



"*Impact of scaling on the soft error sensitivity of bulk, FDSOI and FinFET technologies due to atmospheric radiation*", G. Hubert, L. Artola and D. Regis, Integration the VLSI journal, vol. 50, pp. 39-47, 2015.

Summary and conclusions

- Device level resiliency can be *reasonably* computed
- Simulation tools at different levels offer valuable insight
- Methodology is well-accepted in the community
  - Allows to sneak peek into current and future technology

Part #2

Device Level Resilience

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Where to start looking… (1)

- Taxonomy
  - "*A survey on fault injection methods of digital integrated circuits*", M. Eslami, B. Ghavami, M. Raji, A. Mahani, Integration, v. 71, 2020, pp. 154-163
- Beaming
  - "*Impact of scaling on the soft error sensitivity of bulk, FDSOI and FinFET technologies due to atmospheric radiation*", G. Hubert, L. Artola and D. Regis, Integration the VLSI journal, vol. 50, pp. 39-47, 2015.
  - "*Analysis of Neutron-Induced Multibit-Upset Clusters in a 14-nm Flip-Flop Array*", S. Kumar et al., in IEEE Transactions on Nuclear Science, vol. 66, no. 6, pp. 918-925, June 2019
- Spice methodology
  - "*A Detailed Methodology to Compute Soft-Error Rates in Advanced Technologies*", M. Riera, R. Canal, J. Abella, A. Gonzalez, DATE'16, March 2016

Where to start looking… (2)

- HDL simulation/emulation
  - "*Error injection-based study of soft error propagation in AMD Bulldozer microprocessor module*", C. Constantinescu, M. Butler and C. Weller, DSN 2012
  - "*Soft Error Sensitivity Evaluation of Microprocessors by Multilevel Emulation-Based Fault Injection*", L. Entrena, M. Garcia-Valderas, R. Fernandez-Cardenal, A. Lindoso, M. Portela and C. Lopez-Ongil, in *IEEE Transactions on Computers*, vol. 61, no. 3, pp. 313-322, March 2012
  - "*Enhancement of Fault Injection Techniques Based on the Modification of VHDL Code*", J. Baraza, J. Gracia, S. Blanc, D. Gil and P. Gil, in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 16, no. 6, pp. 693-706, June 2008
- Analytical software
  - "*MASkIt: Soft Error Rate Estimation for Combinational Circuits*", M. Anglada, R. Canal, J. L. Aragón, A. González, ICCD-34, October 2016
  - "*SRAM Memory Margin Probability Failure Estimation using Gaussian Process Regression*", M. Rana, R. Canal, J. Han, B. Cockburn, ICCD-34, October 2016
  - "*Using Boolean satisfiability for computing soft error rates in early design stages*", S.Z. Shazli, M.B. Tahoori, Microelectronics Reliability, v.50 n. 1, 2010, pp. 149-159
  - "*A SET propagation EDA tool based on analytical glitch propagation model*", S. Barceló, X. Gili, S. A. Bota and J. Segura, 14th European Conference on Radiation and Its Effects on Components and Systems (RADECS), Oxford, 2013

Where to start looking… (3)

- TVF numbers presented:
  - "A Detailed Methodology to Compute Soft-Error Rates in Advanced Technologies“, M. Riera, R. Canal, J. Abella, A. Gonzalez, DATE’16, March 2016
  - "*Impact of scaling on the soft error sensitivity of bulk, FDSOI and FinFET technologies due to atmospheric radiation*“, G. Hubert, L. Artola and D. Regis, Integration the VLSI journal, vol. 50, pp. 39-47, 2015.

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